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10/613,212	07/07/2003	Youichi Tobita	57454-966	4586

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,212	TOBITA, YOUICHI	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In communication dated, December 12th, 2005 the applicant: supplied additional drawings figures 9-11, amended the specification to support the additional figures, traversed the rejection of claims 1-9 and drafted two new claims, 10 and 11. Currently claims 1-11 are pending.

Drawings

2. Applicant's new drawings, figures 9-11, have not added any new matter and have affected a better understanding of the invention. Therefore, the previous drawing objection is withdrawn.

Response to Arguments

3. Applicant's arguments filed December 12th, 2005 have been fully considered but they are not persuasive.

4. On page 12 of the Applicant's remarks, the Applicant argues that Shimada does not disclose all of the limitations of claims 1 and 9. Specifically applicant claims that Shimada does not disclose use of, "a voltage of said second gate line in said non-select state to a third voltage that is intermediate between a maximum value and a minimum value of said display voltage."

Examiner respectfully disagrees. As previously cited, a clear picture of the voltage waveforms applied to the transistor gates of Shimada is illustrated in figure 7. The waveforms read on claims 1 and 9 as follows, the first voltage is equivalent to the On-Period of G(1,1) and G(1,2), the second voltage is equivalent to the Off-Period of the First Field of G(1,1), and the third voltage is equivalent to the Off-Period of the First

Field of G(1,2). This third voltage is clearly intermediate between a maximum value (On-Period) and a minimum value (Off-Period of Second Field of G(1,2)).

Additionally, Shimada assumes a video display signal of ±6 V (col. 4, line 4). As shown in figure 5, Vgs' is equivalent to the third voltage. Shimada also discloses a base Vgs value of 0 volts, equivalent to the second voltage. As further shown in figure 5, Vgs'=Vgs+X. One optional value for X is 3 volts, which would clearly create a Vgs' value that is intermediate a max. and min. of the display voltage of ±6 volts (for further explanation see cols. 3 and 4).

5. On page 13 of the Applicant's remarks, the Applicant argues that the invention of Shimada differs from the Applicant's invention claimed in claims 1 and 9 in that the third voltage can be constant voltage among fields as shown in expressions 14 and 17 of the Applicant.

The Examiner respectfully disagrees, it is noted that the feature upon which applicant relies (a constant third voltage amongst different fields) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Additionally the Applicant themselves admit that this feature is merely a possibility and is not required based on the currently claimed invention, by stating: "the third voltage that is the gate voltage in a non-select state *can be* a constant voltage among fields" (emphasis added).

6. The Applicant's argument at the bottom of page 13 and top of page 14 are drawn to further features that the Applicant argues that Shimada does not disclose. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., alleviating voltage stress to a gate insulation film) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As Shimada fully teaches applying a "third voltage that is intermediate between a maximum value and a minimum value of said display voltage", the rejections of claims 1 and 9 are appropriate.

7. The Applicant's additional arguments stating dependent claims 5-7 are allowable simply due to their inclusion of the limitations of claim 1 (page 14), are moot in view of Shimada teaching all of the claimed limitations of claim 1.

8. The Applicant's additional arguments stating dependent claims 2-4 and 8 are allowable simply due to their inclusion of the limitations of claim 1 (page 14), are moot in view of Shimada teaching all of the claimed limitations of claim 1.

With regards to new claims 10 and 11, see the below rejections.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 10 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 10 and 11 are drawn to a constant third voltage among fields. In the Applicant's remarks, the Applicant states that there is support for these claims in expressions 14 and 17 of the specification. Examiner respectfully disagrees. There is never any mention of the variability or the constancy of the third voltage, in the expressions or throughout the specification. Also there is never any mention of fields or frames of any sort in the application as originally filed.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 5-7, and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (US 5,506,598).

With respect to claim 1, Shimada discloses, a liquid crystal display apparatus comprising: a plurality of pixels arranged in rows and columns, each for providing luminance corresponding to a display voltage; (fig. 2)

a plurality of first gate lines provided corresponding to respective said rows of said plurality of pixels; (G(1,1) and G(2,1) in fig. 2)

a plurality of second gate lines provided corresponding to respective said rows of said plurality of pixels; (G(1,2) and G(2,2) in fig. 2)

a plurality of data lines provided corresponding to respective said columns of said plurality of pixels; (102 in fig. 2)

a gate drive circuit for driving each of said plurality of first and second gate lines to a voltage that is different between a select state in which corresponding one of said rows is selected for a scanning target in accordance with a prescribed scanning cycle and a non-select state except for said select state; (109 in fig. 2)

and a source drive circuit for driving said plurality of data lines to said display voltage that corresponds to the pixels included in the row selected for said scanning target; (108 in fig. 2)

said plurality of pixels each including a liquid crystal element having a pixel electrode and a common electrode for providing luminance that corresponds to a voltage difference between said pixel electrode and said common electrode, (107 in fig. 2)

a first field-effect transistor electrically connected between corresponding one of said data lines and a first node, and having its gate electrically connected to corresponding one of said first gate lines, (103a in fig. 2)

and a second field-effect transistor electrically connected between said first node and said pixel electrode, and having its gate electrically connected to corresponding one of said second gate lines; (103b in fig. 2)

said gate drive circuit setting each voltage of said first and second gate lines in said select state to a first voltage (first field on-period voltage in fig. 7) that can turn-on each of said first and second field-effect transistors, while setting a voltage of said first gate line in said non-select state to a second voltage (G(1,1) first field off-period voltage in fig. 7) that can turn-off said first field-effect transistor as well as setting a voltage of said second gate line in said non-select state to a third voltage (G(1,2) first field off-period voltage in fig. 7, also see col. 3, lines 43-45) that is intermediate between a maximum value and a minimum value of said display voltage (col. 5, lines 53-56; also see the above response to arguments section).

With respect to claim 5, Shimada discloses, the liquid crystal display apparatus according to claim 1 (see above), said gate drive circuit setting said second gate line in the non-select state to said third voltage (G(1,2) first field off-period voltage in fig. 7) in a normal mode, and setting to a sixth voltage (G(1,2) second field off-period voltage in fig. 7) in a test mode, and a difference between said first and sixth voltages being larger than a difference between said first and third voltages (see fig. 7).

With respect to claim 6, Shimada discloses, the liquid crystal display apparatus according to claim 5 (see above), said sixth voltage (G(1,2) second field off-period voltage in fig. 7) being substantially at a same level as said second voltage (G(1,1) first field off-period voltage in fig. 7).

With respect to claim 7, Shimada discloses, the liquid crystal display apparatus according to claim 1 (see above), said first and second field-effect transistors being

formed with an N-type thin film transistor (col. 3, lines 20-23), and said first voltage being higher than said second voltage (see fig. 7).

With respect to claim 9, the limitations of claim 9 are such that claim 9 is rejected on the same merits as those recited in the rejection of claim 1 (see above).

With respect to claim 10, Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada further discloses, that the third voltage (off-period of first field of G(1,2) in fig. 7) is constant among the fields ("Among the fields" is broad terminology. As shown in fig. 7, the third voltage is clearly constant within the first field for transistor G(1,2) and constant once again within the second field for transistor G(1,1). This satisfies the limitation for the third voltage being constant among the fields.).

With respect to claim 11, Shimada discloses the liquid crystal display apparatus according to claim 9 (see above).

Shimada further discloses, that the third voltage (off-period of first field of G(1,2) in fig. 7) is constant among the field ("Among the field" is even broader terminology than that of claim 10. As shown in fig. 7, the third voltage is clearly constant within the first field of G(1,2). This is all that is required to satisfy the limitation that the third voltage be constant among the field.)

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Morozumi et al. (US 4,591,848).

Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said common electrode being supplied with a prescribed DC voltage, and said third voltage being substantially at a same level as said prescribed DC voltage.

Morozumi discloses, said common electrode being supplied with a prescribed DC voltage (col. 8, lines 46-47), and said third voltage being substantially at a same level as said prescribed DC voltage (col. 9, lines 32-33, also see fig. 22).

Shimada and Morozumi are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the common electrode DC voltage as the gate driver voltage, taught by Morozumi, in the drive circuitry of Shimada.

The motivation for doing so would have been to generate a more favorable root-mean-square value of a picture element (Morozumi, col. 9, lines 30-31).

Therefore, it would have been obvious to combine Morozumi with Shimada for the benefit of a more favorable root-mean-square value to obtain the invention as specified in claim 2.

14. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Koden et al. (US 5,465,168).

Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said common electrode being supplied with an AC voltage that is set to one of fourth and fifth voltages in a constant cycle, and said third voltage being substantially at a same level as an average of said fourth and fifth voltage.

Koden discloses, said common electrode being supplied with an AC voltage that is set to one of fourth and fifth voltages in a constant cycle (V1/1 in fig. 12), and said third voltage (0 volts in G1 in fig. 12) being substantially at a same level as an average of said fourth and fifth voltage. (V1/1 average is zero volts).

Shimada and Koden are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the average of the common electrode AC voltage as the gate driver voltage, taught by Koden, in the drive circuitry of Shimada.

The motivation for doing so would have been to generate a more favorable root-mean-square value of a picture element (Morozumi, col. 9, lines 30-38).

Therefore, it would have been obvious to combine Koden with Shimada for the benefit of a more favorable root-mean-square value to obtain the invention as specified in claim 3.

15. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Yumoto (US 2004/0207615).

Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said gate drive circuit including a plurality of drive units provided corresponding to said rows, respectively; said plurality of drive units each including a first driver for driving corresponding one of said first gate lines with one of said first and second voltages in response to a select signal that indicates whether said corresponding one of said rows s selected for said scanning target, and a second driver for driving corresponding one of said second gate lines with one of said first and third voltages in response to said select signal.

Yumoto discloses, said gate drive circuit including a plurality of drive units provided corresponding to said rows (21 and 23 in fig. 7), respectively; said plurality of drive units each including a first driver for driving corresponding one of said first gate lines with one of said first and second voltages in response to a select signal (scanB1...scanBN in fig. 7) that indicates whether said corresponding one of said rows selected for said scanning target, and a second driver for driving corresponding one of said second gate lines with one of said first and third voltages in response to said select signal (scanA1...scanAN in fig. 7).

Shimada and Yumoto are analogous art because they are from the same field of endeavor, namely display gate driver circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the gate drive circuitry of Yumoto with the pixel configuration and voltage levels of Shimada.

The motivation for doing so would have been to effectively generate the plurality of voltages that are implemented in Shimada.

Therefore, it would have been obvious to combine Morozumi with Shimada for the benefit of effectively generating voltages to obtain the invention as specified in claim 4.

16. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Kondo et al. (US 6,313,818).

Shimada discloses the liquid crystal display apparatus according to claim 1 (see above).

Shimada does not expressly disclose said first and second field-effect transistors being formed with a P-type thin film transistor, and said first voltage being lower than said second voltage.

Kondo discloses, said first and second field-effect transistors being formed with a P-type thin film transistor, and said first voltage being lower than said second voltage (col. 2, lines 14-20).

Shimada and Kondo are analogous art because they are from the same field of endeavor, namely active-matrix liquid crystal display devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the N-type transistors of Shimada with the P-type transistors of Kondo.

The motivation for doing so would have been gain the benefit of a smaller subthreshold leakage current.

Therefore, it would have been obvious to combine Kondo with Shimada for the benefit of smaller leakage currents to obtain the invention as specified in claim 8.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 8:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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1/3/06

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